

Institute for Complex Systems (ICS)



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System-on-Chips (SoCs)

- Omnipresent
- Increasingly complex systems
- In particular SW importance/complexity rising rapidly:
 - ASIC era: SW was afterthought
 - SoC era: SW is integral part
 - Bootcode, device driver, firmware, OS, libraries (network stack), application
- **Problem:**
Traditional design flow (first HW then SW) insufficient

```
string sInput;  
int iLength, iN;  
double dblTemp;  
bool again = true;
```

```
while (again) {  
    iN = -1;  
    again = false;  
    getline(cin, sInput);  
    system("cls");  
    stringstream(sInput) >> dblTemp;  
    iLength = sInput.length();  
    if (iLength < 4) {  
        again = true;  
        continue;  
    } else if (sInput[iLength - 3] != '.') {  
        again = true;  
        continue;  
    } while (++iN < iLength) {  
        if (isdigit(sInput[iN])) {  
            continue;  
            if (iN == (iLength - 3)) {
```



... and Verification?

- Design already hard!
- **New approaches to verify cooperation of SW and HW needed!**
 - Application SW has to exploit cores & IPs
- **@ICS:**
 - Design & verification flow starting from **Virtual Prototype (VP)** down to **HW**
 - Core concept: abstraction
 - HW/SW no longer two worlds
 - Verification happens earlier, with less irrelevant detail



Open source and collaboration
are strategic to software and hardware
across industries and geographies.



Disruptive Technology

Barriers

	Legacy ISA	RISC-V ISA
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	\$\$\$ – Limited	Free – Unlimited
License and Royalty fees	\$\$\$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions and cores. More design companies on RISC-V than any other architecture
Software ecosystem	Extensive	Growing rapidly. Easy to compile for RISC-V

RISC-V Foundation Members (>1000 today)



RISC-V News

- **Prediction:** More than 64 billion RISC-V cores by 2025 (Semico Research Corp.)

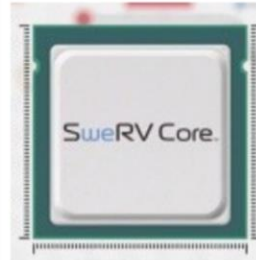


SMARTPHONES **UPDATE**

Qualcomm nutzt RISC-V in Snapdragon-Chips

Einer der größten SoC-Entwickler setzt mittlerweile auf RISC-V: Qualcomm integriert Kerne mit der offenen Befehlssatzarchitektur für den Embedded-Einsatz in aktuellen und zukünftigen Snapdragon-Chips.

24.01.2020 4 Kommentare



SAMSUNG & WESTERN DIGITAL

RISC-V-Kerne für 5G-mmWave und SSDs

Die offene CPU-Befehlssatzarchitektur RISC-V gewinnt an Verbreitung: Samsung verwendet entsprechende Kerne für 5G-mmWave-Module und Western Digital hat zwei weitere Designs für SSD-Controller.

16.12.2019 0 Kommentare

news

CHIPGIGANT ARM

Poker um Deal mit weltweiten Folgen

Ein geplanter Megadeal in der Chipbranche sorgt für Kritik von Wettbewerbshütern auf der ganzen Welt: Das US-Unternehmen Nvidia will den britischen Chipdesigner Arm kaufen, dessen Technologie den Kern jedes modernen Smartphones bildet. Bisher gehörte Arm dem japanischen Telekomkonzern SoftBank und galt damit praktisch als „neutral“ – dass Arm nun in US-Hand kommen soll, beunruhigt nicht nur China.

8. September 2021, 18.52 Uhr

Teilen

Worst-Case-Szenario als Chance für offene Alternative

Sollte die Übernahme von Arm durch Nvidia tatsächlich Auswirkungen auf die weltweite Rechnerproduktion haben, könnte das – zumindest längerfristig – dazu führen, dass sich Hersteller nach Alternativen zu den Arm-Designs umsehen. Einen Kandidaten – bisher grober Außenseiter – gibt es dafür schon. **Mit RISC-V existiert ein Konkurrenzstandard mit einem enormen Vorteil: Die Rechnerarchitektur ist offen verfügbar – das heißt, für die Verwendung in Chips fällt an sich keine Lizenzgebühr an.**

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Intel Offers \$2 Billion for RISC-V Chip Startup SiFive: Bloomberg

By [Paul Alcorn](#) June 10, 2021

Technology

Intel and Softbank Beware. Open Source Is Coming to the Chip Business

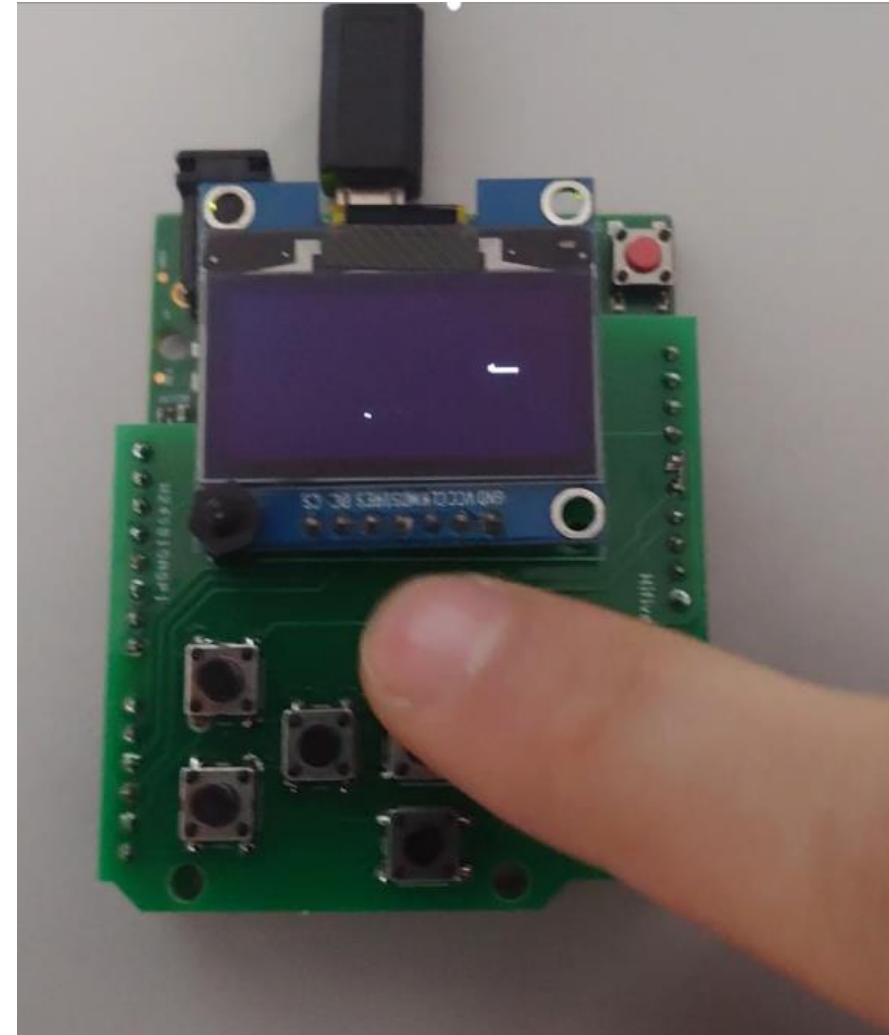
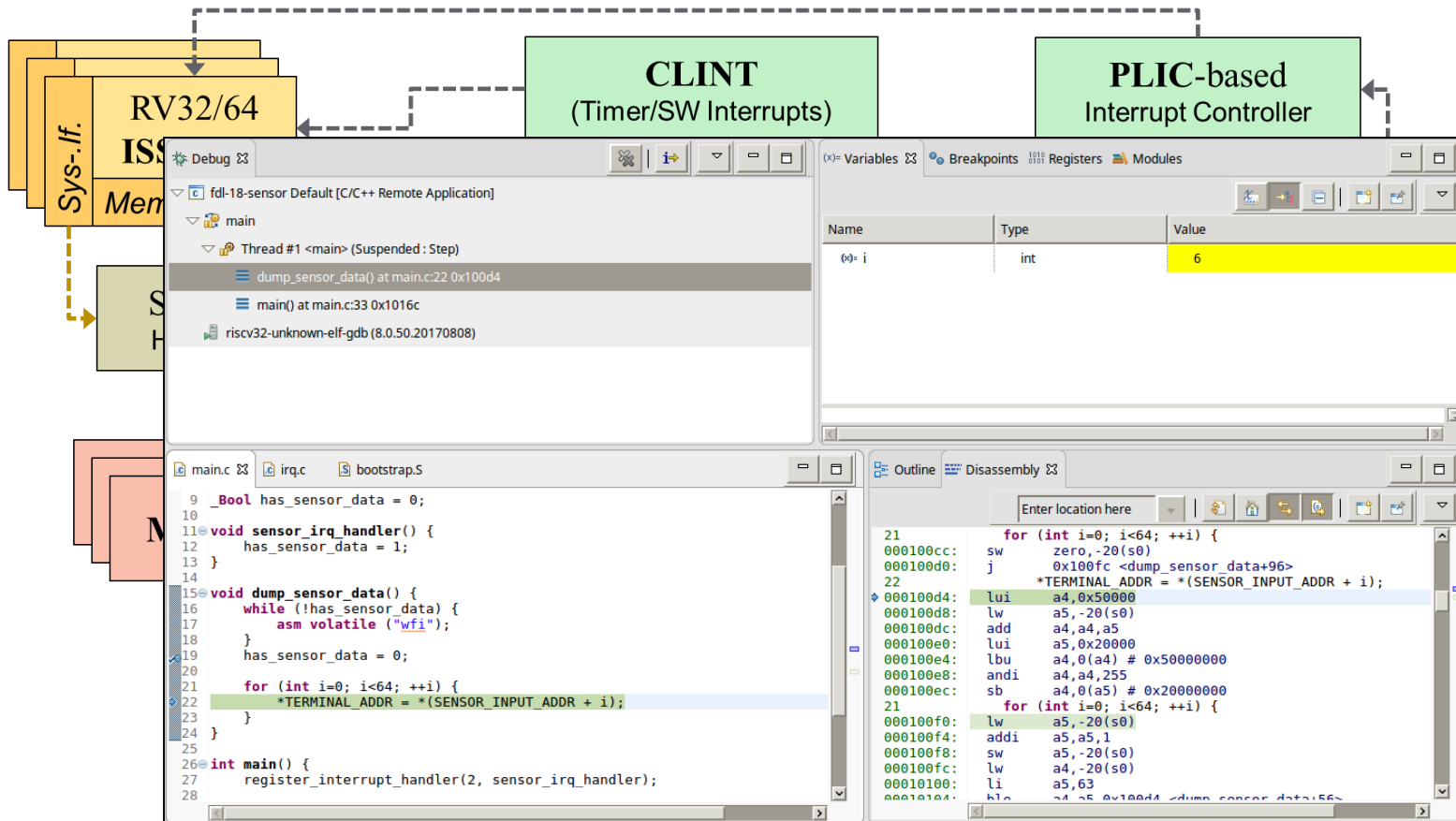
By [Ian King](#)

22. Januar 2020, 15:00 MEZ

@ICS: Open Source RISC-V VP

VP Architecture

→ TLM2.0 generic payload - - -> Interrupt Interface - - -> Syscall Interface

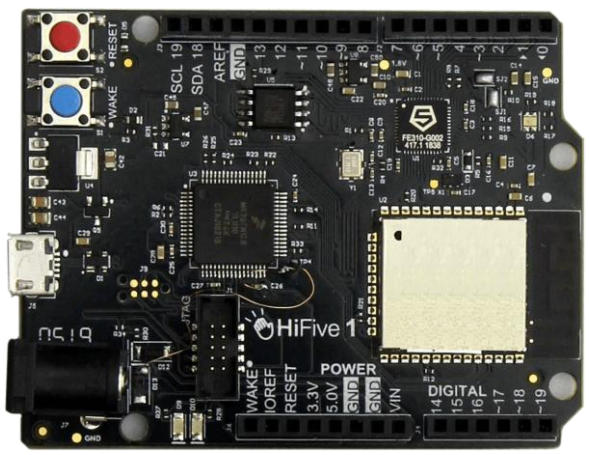
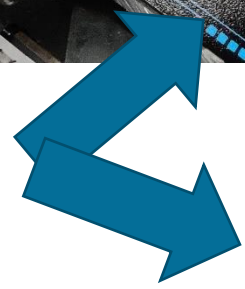
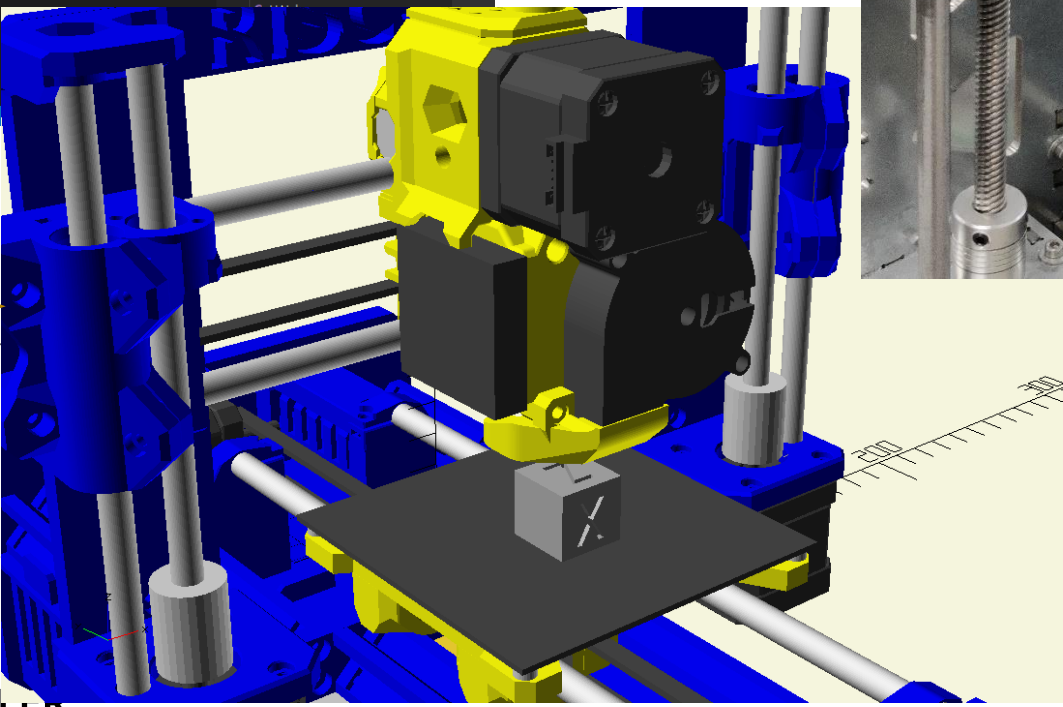
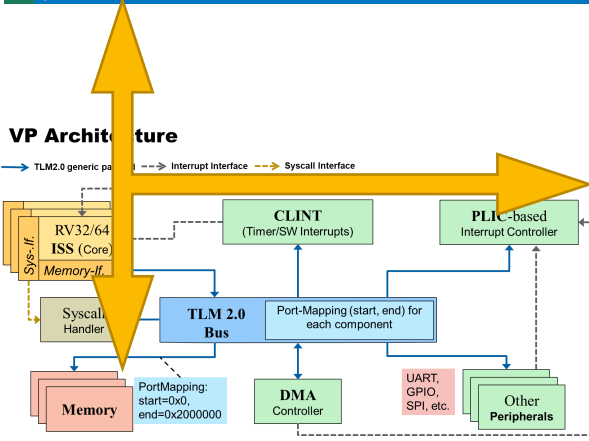
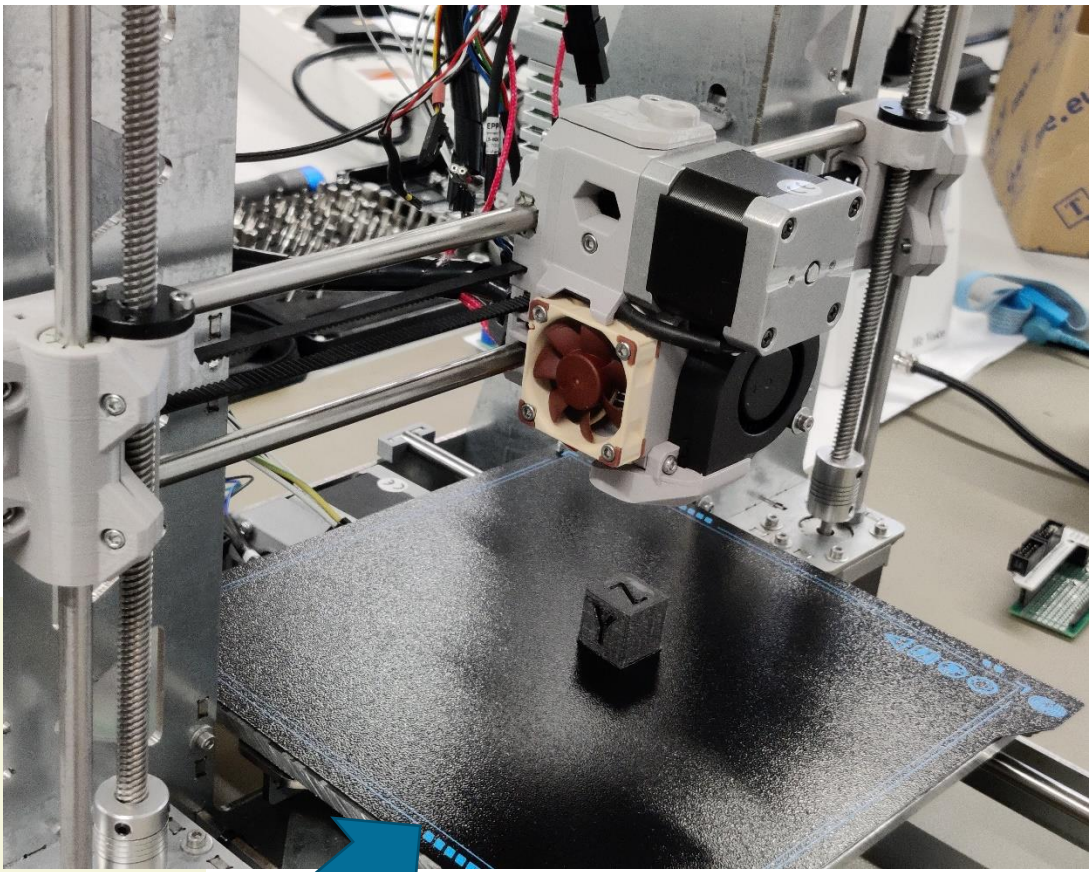



```

watchdog.cpp - marlin - Visual Studio Code
File Edit Selection View Go Run Terminal Help
C uart.h U G uart.cpp U G MarlinSerial.cpp M {} launch.json M G watchdog.cpp X PIC ... EXPLORER
Marlin > src > HAL > AVR > G watchdog.cpp > ...
30 #include "../MarlinCore.h"
31
32 // Initialize watchdog with 8s timeout, if possible. Otherwise, make it 4s.
33 void watchdog_init() {
34   #if ENABLED(WATCHDOG_DURATION_8S) && defined(WDTO_8S)
35     #define WDTO_NS WDTO_8S
36   #else
37     #define WDTO_NS WDTO_4S
38   #endif
39   #if ENABLED(WATCHDOG_RESET_MANUAL)
40     // Enable the watchdog timer, but only for the interrupt.
41     // Take care, as this requires the correct order of operation, with interrupts disa
42     // See the datasheet of any AVR chip for details.
43     wdt_reset();
44     cli();
45     _WD_CONTROL_REG = _BV(_WD_CHANGE_BIT) | _BV(WDE);
46     _WD_CONTROL_REG = _BV(WDIE) | (WDTO_NS & 0x07) | ((WDTO_NS & 0x08) << 2); // WDTO_N
47     sei();
48     wdt_reset();
49   #else
50     wdt_enable(WDTO_NS); // The function handles the upper bit correct.
51   #endif
52 }
53 //delay(10000); // test it!

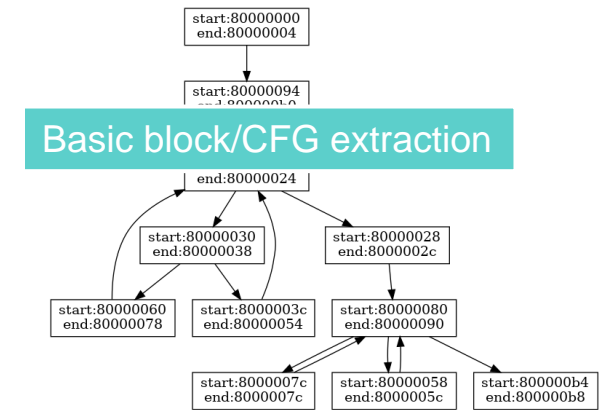
```

hazott@hazott-ThinkPad-T14-Gen-1:~/Projects/riscv3dp/software/sw/marlin\$



WAL: Waveform Analysis Language

- Waveform debugging
 - Tedious and slow
 - Manual
 - Can not be automated
 - Or can it?
- WAL is *Domain Specific Language* (DSL) to express waveform analysis problems



318	lw x3, 0(x1)	addi x2, x2, 40	auipc x2, 1	addi x1, x1, 0
320	addi x4, x3, 1	lw x3, 0(x1)	addi x2, x2, 40	auipc x2, 1
322	addi x4, x3, 1	addi x4, x3, 1	lw x3, 0(x1)	addi x2, x2, 40
324	addi x4, x3, 1	addi x4, x3, 1	addi x4, x3, 1	lw x3, 0(x1)
326	flush	flush	flush	flush

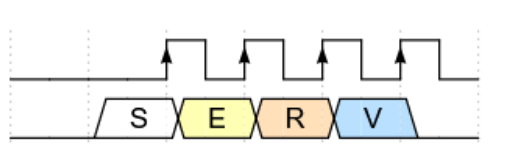
Warning 1: Pipeline flushed, current instruction lw x3, 0(x1) Previous Next

328	addi x4, x3, 1	addi x4, x3, 1	addi x4, x3, 1	lw x3, 0(x1)
330	addi x5, x3, 2047	addi x4, x3, 1	addi x4, x3, 1	addi x4, x3, 1
332	lw x3, 0(x1)	addi x5, x3, 2047	addi x4, x3, 1	addi x4, x3, 1
334	addi x4, x3, 1	lw x3, 0(x1)	addi x5, x3, 2047	addi x4, x3, 1
336	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)	addi x5, x3, 2047
338	addi x4, x3, 1			0(x1)
340	addi x4, x3, 1			0(x1)
342	addi x4, x3, 1			0(x1)
344	addi x4, x3, 1			0(x1)
346	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)	lw x3, 0(x1)
	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)	lw x3, 0(x1)
	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)	lw x3, 0(x1)
	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)	lw x3, 0(x1)
	addi x4, x3, 1	addi x4, x3, 1	lw x3, 0(x1)	lw x3, 0(x1)

Pipeline status visualization

Warning 1: Pipeline halted for 11 cycles, current instruction lw x3, 0(x1) Previous Next

addi x4, x3, 1	addi x4, x3, 1	addi x4, x3, 1	lw x3, 0(x1)
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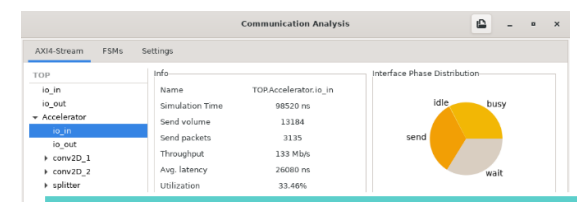


Du hast retweetet

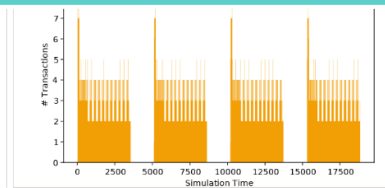
Olof Kindgren @OlofKindgren · 21. Jan.

So, @lcsklmmr and @Daniel_Grosse made a DSL called WAL for analysing waveforms. Now what can you do with such a thing? Well, for one you can calculate how many cycles it takes for SERV to execute each instruction. Check it out here

LucasKI/serv-cpi



Throughput, Latency on AXI bus



Areas

- Modelling & Implementation of FPGAs
 - RISC-V cores
 - Accelerators (NNs, Approximate Computing)
 - ...

- Verification
 - Fuzzing
 - Metamorphic Testing
 - Symbolic execution of SW interacting w HW
 - Symbolic Computer Algebra (SCA) for hard arithmetic (e.g. multipliers) at gate level
 - ...

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