ICS
Institute for Complex Systems

DI Manfred Schlägl
Head: Univ.-Prof. Dr.-Ing. Daniel Große
jku.at/ics

JOHANNES KEPLER UNIVERSITY LINZ

System-on-Chip (SoC)

- Omnipresent + very complex
- Heart: **Processor**
  - Very hot: RISC-V

Android für RISC-V: Google präzisiert Pläne

Vor fast einem Jahr hatte Google erstes Interesse gezeigt, Android auf die RISC-V-Architektur zu portieren, nun folgen erste Ergebnisse.

Lesezeit: 1 Min. In Pocket speichern 3

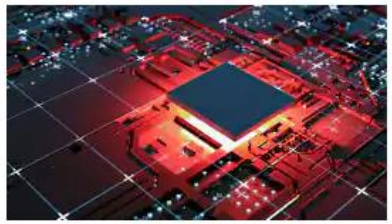
RISC-V-Kerne in gängigem Chip-Entwicklerwerkzeug von Synopsys integriert

Synopsys, der große Anbieter von Software für Chipdesigner (EDA-Tools), offeriert nun auch RISC-V-Kerne mit 32 oder 64 Bit zum SoC-Einbau.

Lesezeit: 2 Min. In Pocket speichern

31.10.2023 17:36 Uhr | c't M

Von Jörg Wirtgen



OpenAI will für 51 Millionen US-Dollar neuromorphe Chips kaufen

Die Rain-NPU soll **RISC-V**-Prozessorkerne mit integriertem Resistive RAM (ReRAM oder RRAM) kombinieren....

04.12.2023 | heise online

Synopsys ARC-V: Eingebettete RISC-V-Kerne (Bild: Synopsys)

08.11.2023 11:55 Uhr | c't Magazin

Von Christof Windeck

US Edition

Intel C ... artup

SiFive: Bloomberg

By Paul Alcorn June 10, 2021

c't magazin für computer technik

RISC-V-Prozessoren fliegen in Weltraum

12.09.2022 18:08 Uhr Christof Windeck

Die NASA setzt beim High-Performance Spaceflight Computing (HPSC) künftig auf RISC-V. Ein europäischer Nanosat mit RISC-V-CPU umkreist bereits die Erde.

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- Heart: **Processor**
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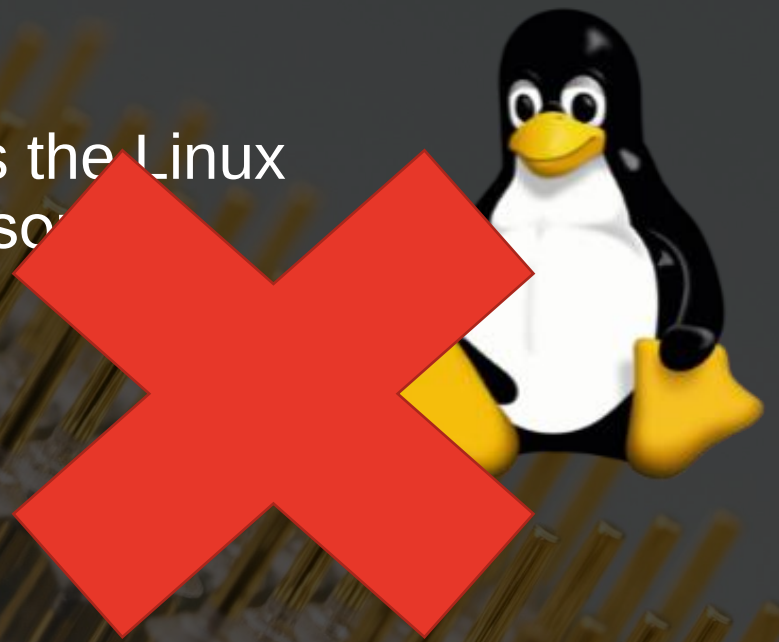
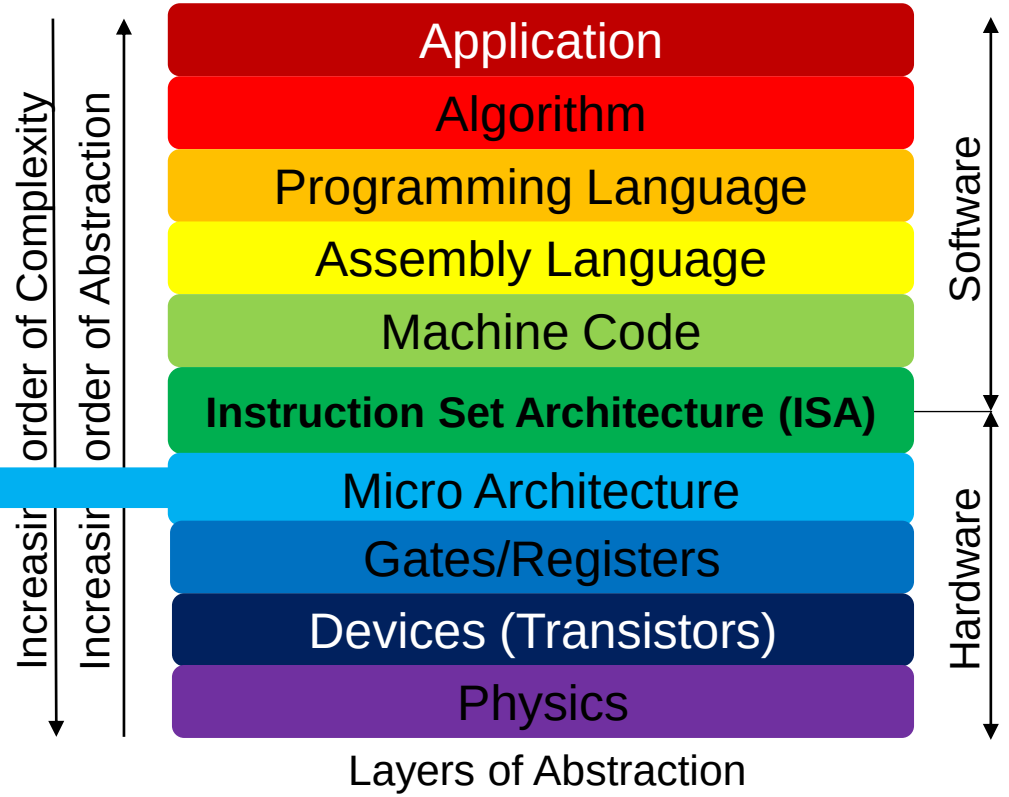
“RISC-V is the Linux
of processo



Instruction Set Architecture (ISA)

- Instruction Set Architecture (ISA)

  is the interface between HW and SW
  - Instructions (encoding & semantics)
  - Number and types of registers
  - Memory access, addressing modes



Modular Design

Intel x86, ARM
Incremental instruction set

RISC-V
Composable extensions

Disruptive **Technology**

Barriers	Legacy ISA	RISC-V ISA
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions and cores. More design companies on RISC-V than any other architecture
Software ecosystem	Extensive	Growing rapidly. Easy to compile for RISC-V
Specification	180 hours to read	6 hours to read

RISC-V®

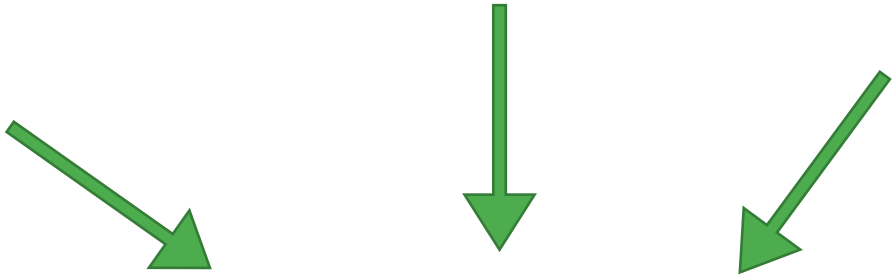
RISC-V is an open standard

Bachelor Thesis

I want to implement an AI accelerator!

I want to work on SW side or programming languages!

I want to implement my own processor!

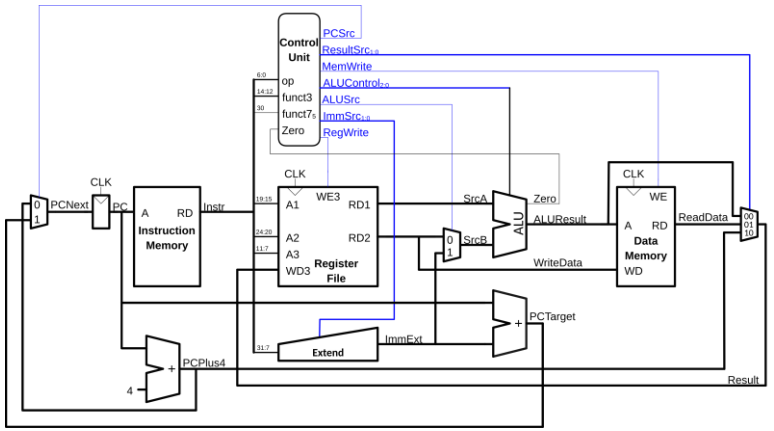


Contact us

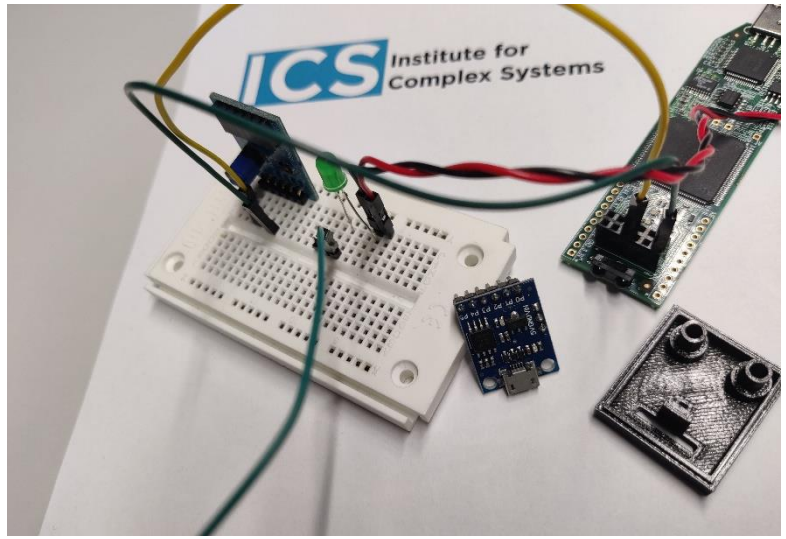
- **Together** we will work out the topic of your thesis
- Depending on **your** interests
- Already have an idea? Great!
- We support you at every stage of your thesis

A very cool result
And a new title for your collection

Research Areas at our Institute

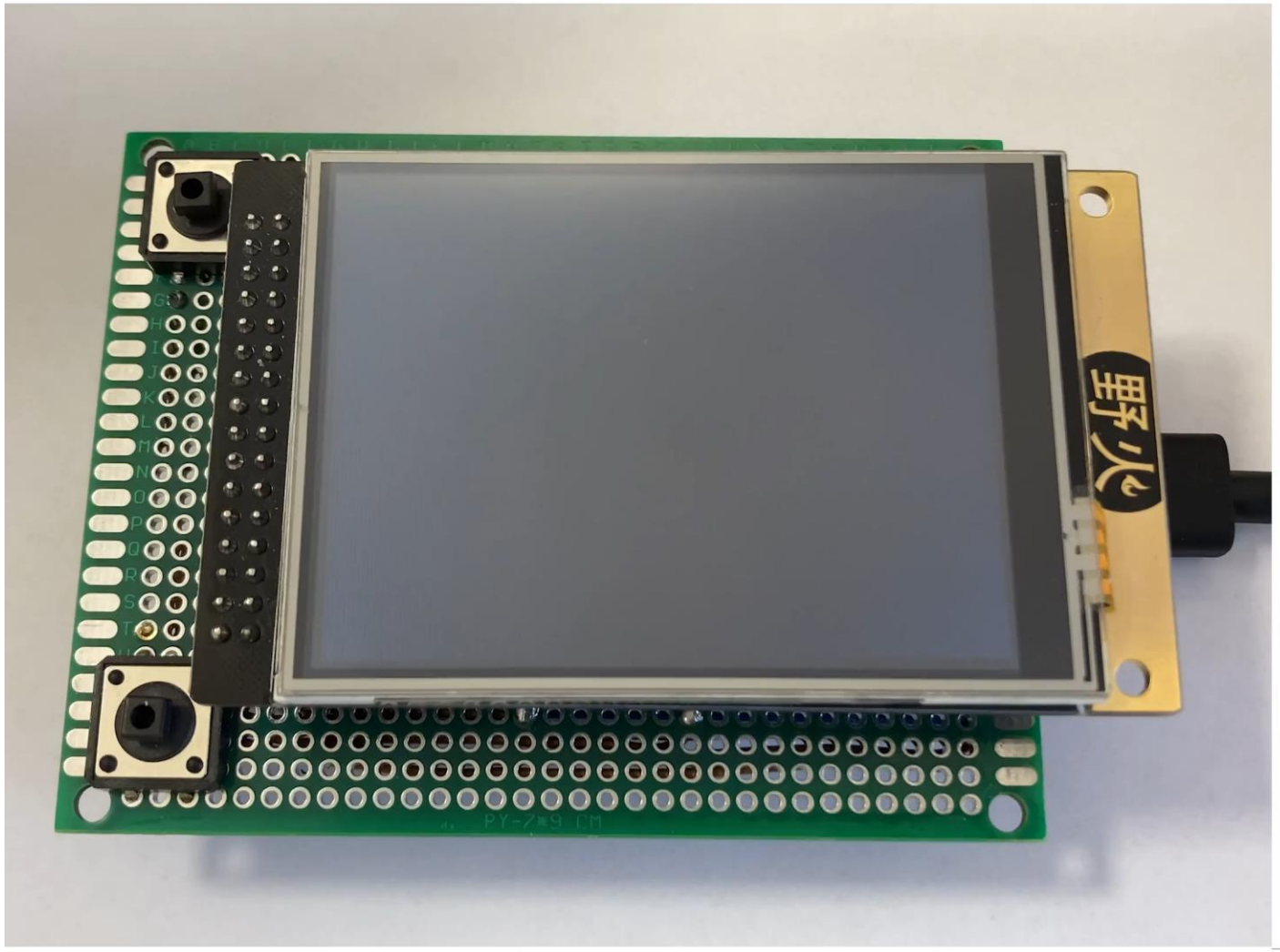


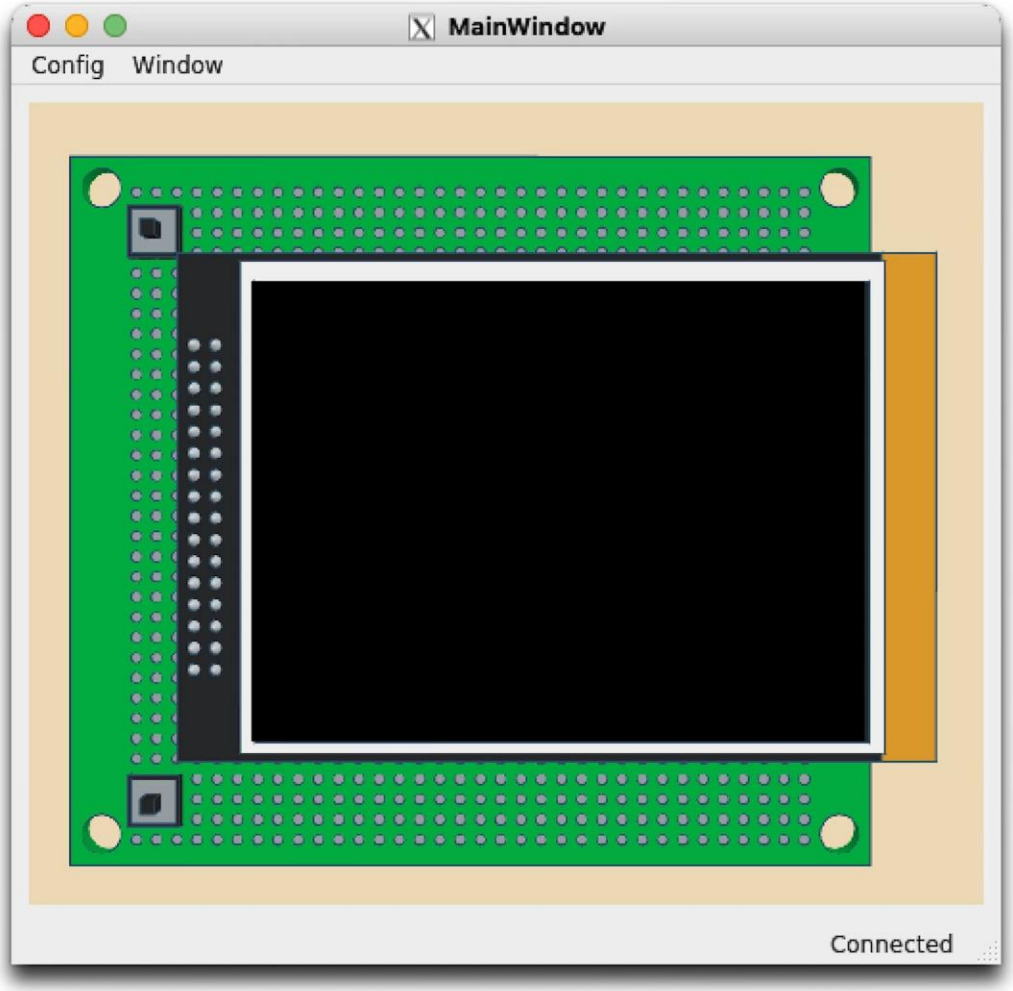
- Modelling & Implementation
  - RISC-V virtual prototypes
  - RISC-V cores (VHDL, Verilog)
  - SUBLEQ Processor (processor in 1 instruction)
  - Accelerators (RISC-V Vector extension, NNs, Approximate Computing)
  - …
- Electronic Design Automation: e.g. verification
  - Property Checking / Equivalence Checking
  - Waveform Analysis Language (WAL)
  - Fuzzing
  - Metamorphic Testing
  - Symbolic execution of SW interacting with HW
  - Symbolic Computer Algebra (SCA) for hard arithmetic (e.g. multipliers) at gate level



→ **More Details:** https://ics.jku.at/research/

Metamorphic Testing and Virtual Prototypes





Institute for Complex Systems

Contact us!

- **Univ.-Prof. Dr. Daniel Große**
- **Science Park 4, 3rd floor**
- **daniel.grosse@jku.at**
- **jku.at/ics**

Bachelor- and Masterthesis
https://ics.jku.at/teaching/theses/

also: Seminars / Projects

Target: Mastering the constantly growing complexity of hardware/software systems

Topics:
- Virtual Prototypes (VPs) for HW/SW systems (System Level)
- HW designs in Verilog/VHDL at the Register Transfer Level (RTL), down to the gate-level

Primary research areas:
- Verification, debugging, and synthesis
- Problems in Electronic Design Automation (EDA)

We heavily use RISC-V in our research work (see e.g. our open-source RISC-V VP++).

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